# Koneru Lakshmaiah Education Foundation

(Category -1, Deemed to be University estd. u/s. 3 of the UGC Act, 1956)

Accredited by **NAAC** as 'A++' ❖ Approved by AICTE ❖ ISO 21001:2018 Certified

**Campus:** Green Fields, Vaddeswaram - 522 302, Guntur District, Andhra Pradesh, INDIA.
Phone No. +91 8645 - 350 200; www.klef.ac.in; www.klef.edu.in; www.kluniversity.in

**Admin Off:** 29-36-38, Museum Road, Governorpet, Vijayawada - 520 002. Ph: +91 - 866 - 3500122, 2576129

**25-04-2020**

**Webinar**
**on**
**"Introduction to Mixed Signal Verification Using Verilog AMS"**

## Circular:

4/3/24, 3:26 PM                                   Mail - HOD-ECE - Outlook

Alumni Webinar (1) on "Introduction to Mixed Signal Verification Using Verilog AMS" on 25-04-2020, ECE Dept.-Reg.

HOD-Department of Electronics and Communication Engineering <hod.ece@kluniversity.in>
Fri 24-04-2020 10:32
To:ECE Faculty <ecefaculty@kluniversity.in>;deanengg@klh.edu.in <deanengg@klh.edu.in>;ecehod@klh.edu.in <ecehod@klh.edu.in>;koteswararao@klh.edu.in <koteswararao@klh.edu.in>;KLH Director <director@klh.edu.in>;ALL HODS <hods@kluniversity.in>;All Deans <deans@kluniversity.in>;Suman Maloji <suman.maloji@kluniversity.in>; madansa@synopsys.com <madansa@synopsys.com>
Cc:PRINCIPAL - COE <principal.coe@kluniversity.in>;Vice Chancellor - KLU <vc@kluniversity.in>;PRESIDENT <president@kluniversity.in>

📎 1 attachments (392 KB)
Alumni Webinar 1.jpg;

Respected Sir/Madam,

After successful kick-start of faculty webinar series, the department is pleased to offer an Alumni Webinar Series with the willing proposals from some of our alumni. In fact, University's alumni are the reflection of its past, representation of its present and a link to its future. They are our most loyal supporters and our best ambassadors, offering invaluable marketing and promotion across their personal and professional networks.

It is also a good idea to share the experiences, present advancements in technology, industry requirements with the teachers who are the career builder for the present students of the University. The shared experiences from the alumni will enlighten our faculty to mold the students for a successful career ahead.

Keeping this in mind, we plan a series of webinars for students and faculty anticipating that it would certainly build a strong and a positive relationship with the alumni benefiting the university or department socially, academically and professionally.

**Webinar:** "Introduction to Mixed Signal Verification Using Verilog AMS"

**Speaker:** Mr. G. Madan Sankar Reddy, Application engineer, SYNOPSYS

**Batch:** 2014-16, M.Tech, ECE Dept.

**Alumni Webinar :** 01

**Date:** 25-04-2020

**Time:** 09 AM

**Register Here:**

https://forms.gle/Wf8KspgZELHtV3Xz8

**Poster:**



**Fig.** Poster of webinar

## 1. Objective and discussions:

Mixed-signal verification using Verilog-AMS (Analog Mixed-Signal) involves verifying designs that contain both analog and digital components. Verilog-AMS is an extension of the Verilog hardware description language (HDL) that allows designers to model mixed-signal systems, including analog behavior.

Here's an introduction to mixed-signal verification using Verilog-AMS:

Verilog-AMS Basics: Verilog-AMS combines the capabilities of Verilog for digital modeling with additional constructs for analog and mixed-signal modeling. It allows designers to describe analog behavior using continuous-time signals and digital behavior using discrete events.

Mixed-Signal System Modeling: Verilog-AMS enables the modeling of mixed-signal systems, which contain both analog and digital components. Analog components can include voltage sources, resistors, capacitors, and transistors, while digital components can include logic gates, flip-flops, and other digital building blocks.

Verification Challenges: Mixed-signal designs pose unique verification challenges due to the interaction between analog and digital components. Verifying such systems requires ensuring that both the analog and digital parts of the design work together correctly under various operating conditions and corner cases.

Verification Techniques: Various verification techniques can be applied to mixed-signal designs using Verilog-AMS:

Analog Behavioral Modeling (ABM): Analog behavior can be modeled using behavioral constructs such as behavioral voltage sources, behavioral capacitors, and behavioral resistors.

Mixed-Signal Co-Simulation: Verilog-AMS allows co-simulation of analog and digital parts of the design, enabling designers to simulate the entire mixed-signal system and analyze its behavior.

Parameter Sweeping: Parameter sweeping techniques can be employed to explore the design space and verify the robustness of the mixed-signal system across different parameter values.

Formal Verification: Formal verification techniques can be used to formally verify properties of the mixed-signal design, such as correctness of analog-to-digital (ADC) and digital-to-analog (DAC) conversions, stability of feedback loops, and compliance with specifications.

Verification Environment Setup: Setting up a verification environment for mixed-signal designs involves creating testbenches that stimulate the inputs of the design and monitor its outputs. This may include generating analog stimulus waveforms, applying digital input sequences, and analyzing the response of the system.

Tool Support: Several EDA (Electronic Design Automation) tools provide support for mixed-signal verification using Verilog-AMS, including simulation tools, formal verification tools, and mixed-signal verification environments.

In summary, mixed-signal verification using Verilog-AMS involves modeling both analog and digital behavior within the same framework, employing various verification techniques to ensure the correctness and robustness of mixed-signal designs.

**Online Link**

https://us02web.zoom.us/j/23543678345633?pwd=dngeertndgksKKYBDerGD09

**Number of participants: 89**

**Fig. List of participants**

**List of the Participated Students: 42**

| S. No. | Roll No | Name |
|--------|---------|------|
| 1 | 180040046 | VOLETI VENKATA SAI  VARUN |
| 2 | 180040150 | AUTHU  SURESH REDDY |
| 3 | 180040278 | SAMMETA  SIREESHA |
| 4 | 180040601 | POTHURI VENKATA DURGA SAI ESWAR |
| 5 | 180040604 | VASIREDDY  BALASARASWATHI |
| 6 | 180040505 | GONGATI   MALLIKHARJUNA REDDY |
| 7 | 180040565 | TEKKAM JEEVANA SRAVANI |
| 8 | 180040615 | PASAM SAI SARAN |
| 9 | 180040029 | BONTHU  LOKESH |
| 10 | 180040502 | PUVVADA VENKATA MADHAVA GUPTA |

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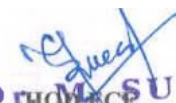
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| 11 | 180040549 | NEKKALAPUDI NIKHILESH RAO |
| 12 | 180040613 | NAGA TEJA |
| 13 | 180040665 | NAKKALA SAI KRISHNA |
| 14 | 180040742 | KANDIKATTU SARANYA |
| 15 | 180040044 | KARETI YASWANTH SAI |
| 16 | 180040102 | JANGALA GIRIDHAR |
| 17 | 180040158 | SHAIK IRFAN AHAMED |
| 18 | 180040215 | BUTHUKURI RAJA SEKHAR REDDY |
| 19 | 180040271 | NEMALI SRINITHYA |
| 20 | 180049013 | KAMBALA JAYA VENKATA SAI PAVAN PHANINDRA |
| 21 | 180040385 | BONDA MANIKANTA SAI SRIRAM |
| 22 | 180040430 | ATLURI HANITH |
| 23 | 180040575 | TELAGAMSETTY BALA VAMSI |
| 24 | 180040671 | AKULA NIVEDITHA |
| 25 | 180040684 | ADABALA N K RAJA RAMESH |
| 26 | 180049010 | KADALI JAGADEESH |
| 27 | 180049012 | KONAKATI SAI KIRAN |
| 28 | 180040231 | TADIKAMALLA V V RANGA NAGA SRI HARSHA |
| 29 | 180040295 | GOWRAV KRISHNA BOYAPATI |
| 30 | 180040670 | NAIDU ANUSH |
| 31 | 180040516 | SAGILI SATYA PRIYA |
| 32 | 180040581 | PAMIREDDYGARI TARUN KUMAR REDDY |
| 33 | 180040422 | GATRAM PANCHAJANYA KUMAR |
| 34 | 180049007 | IRRINKI NAGA DURGA RAJESH |
| 35 | 180040352 | SYED NOOR MOHAMMAD |
| 36 | 180040454 | BATCHU NIKHIL VISHNU |
| 37 | 180040515 | DASARI NIKHITH REDDY |
| 38 | 180040733 | KALYANDEEP PIDIKITI |
| 39 | 180040274 | INAKOLLU KIRAN KUMAR |
| 40 | 180040462 | CHITTURI RAMESH PAVAN KALYAN |
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